WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a first bus;

a processor operable to connect with said first bus;

a first DMA controller operable to connect with said first bus;

a second bus;

a second DMA controller operable to mutually connect said first bus and said second bus;

a first connecting unit comprising a first buffer memory and operable to connect with said second bus; and

a second connecting unit comprising a second buffer memory and operable to connect with said second bus,

wherein said first bus is further operable to connect with a first memory that is externally installed and accessible by said processor, said second bus is further operable to connect with a second memory that is externally installed,

wherein said first DMA controller is operable to arbitrate data transfer between said first memory and said second memory, after requesting said second DMA controller, and

wherein said second DMA controller is operable to arbitrate data transfer between said second memory and said first buffer memory and data transfer between said second memory and said second buffer memory.

2. An integrated circuit as defined in claim 1, wherein said second DMA comprises a DMA arbiter, a transfer output buffer memory and a transfer input buffer memory,

wherein said DMA arbiter, upon receipt of data transfer request from said first connecting unit, arbitrates data transfer between said first buffer memory and said second memory via said second bus,

wherein said DMA arbiter, upon receipt of data transfer request from said second connecting unit, arbitrates data transfer between said second buffer memory and said second memory via said second bus,

wherein said DMA arbiter, upon receipt of data transfer request from said first DMA controller, arbitrates data transfer from said second memory to said first memory via said transfer output buffer memory, and

wherein said DMA arbiter, upon receipt of data transfer request from said first DMA controller, arbitrates data transfer from said first memory to said second memory via said transfer input buffer memory.

3. An integrated circuit as defined in claim 1, wherein said first connecting unit further comprises a connecting circuit that interfaces an external device connected to said first connecting unit with said first buffer memory, and

wherein said second connecting unit further comprises a connecting circuit that interfaces an external device connected to said second connecting unit with said second buffer memory.

4. An integrated circuit as defined in claim 1, wherein said connecting circuit of said first connecting unit and said connecting circuit of said second connecting unit are composed of an FPGA.

5. An integrated circuit as defined in claim 3, wherein said first connecting unit is an image input unit that includes a synchronizing signal detector as said connecting circuit, detects effective image data from an externally inputted image signal, and stores the effective image data to said first buffer memory, and

wherein said second connecting unit is an image output unit that includes a synchronizing signal generator as said connecting circuit, generates image output signal by inserting a synchronizing signal to image data stored in said second buffer memory, and sends externally the image output signal.

6. An integrated circuit as defined in claim 1, wherein said processor is

substituted by a plurality of processors.

7. An image input/output device comprising: an integrated circuit; a first memory; and a second memory,

the integrated circuit comprising:

a first bus;

a processor operable to connect with said first bus;

a first DMA controller operable to connect with said first bus;

a second bus;

a second DMA controller operable to mutually connect said first bus and said second bus;

a first connecting unit comprising a synchronizing signal detector and a first buffer memory and operable to connect with said second bus; and

a second connecting unit comprising a synchronizing signal generator and a second buffer memory and operable to connect with said second bus,

wherein said synchronizing signal detector of said first connecting unit detects effective image data from an externally inputted image signal, and stores the effective image data to said first buffer memory,

wherein said synchronizing signal generator generates image output signal by inserting a synchronizing signal to image data stored in said second buffer memory, and sends externally the image output signal,

the first memory being operable to connect with said first bus and accessible by said processor and said first DMA controller, and

the second memory being operable to connect with said second bus and

accessible by said second DMA controller,

wherein said first DMA controller arbitrates data transfer between said first memory and said second memory, after requesting said second DMA controller, and

wherein said second DMA controller arbitrates data transfer between said second memory and said first buffer memory and data transfer between said second memory and said second buffer memory.

8. An image input/output device as defined in claim 7, wherein said second DMA comprises a DMA arbiter, a transfer output buffer memory and a transfer input buffer memory,

wherein said DMA arbiter, upon receipt of data transfer request from said first connecting unit, arbitrates data transfer between said first buffer memory and said second memory via said second bus,

wherein said DMA arbiter, upon receipt of data transfer request from said second connecting unit, arbitrates data transfer between said second buffer memory and said second memory via said second bus,

wherein said DMA arbiter, upon receipt of data transfer request from said first DMA controller, arbitrates data transfer from said second memory to said first memory via said transfer output buffer memory,

wherein said DMA arbiter, upon receipt of data transfer request from said first DMA controller, arbitrates data transfer from said first memory to said second memory via said transfer input buffer memory.

9. An image input/output device as defined in claim 7, wherein said synchronizing signal detector of said first connecting unit and said synchronizing signal generator in said second connecting unit are respectively composed of an FPGA.

10. An image input/output device comprising: a first integrated circuit; a second integrated circuit; a first memory; and a second memory,

the first integrated circuit comprising:

a first bus;

a processor operable to connect with said first bus;

a first DMA controller operable to connect with said first bus;

a second bus;

a second DMA controller operable to mutually connect said first bus and said second bus;

a first buffer memory operable to connect with said second bus; and

a second buffer memory operable to connect with said second bus;

the second integrated circuit comprising a synchronizing signal detector and a synchronizing signal generator;

the first memory being operable to connect with said first bus and accessible by said processor and said first DMA controller; and

the second memory operable to connect with said second bus and accessible by said second DMA controller,

wherein said synchronizing signal detector and said first buffer memory are mutually connected to form a first connecting unit,

wherein said synchronizing signal generator and said second buffer memory are mutually connected to form a second connecting unit,

wherein said synchronizing signal detector detects effective image data from an externally inputted image signal, and stores the effective image data to said first buffer memory,

wherein said synchronizing signal generator generates image output signal by inserting a synchronizing signal to image data stored in said second buffer memory, and sends externally the image output signal,

wherein said first DMA controller arbitrates data transfer between said first

memory and said second memory through said second DMA controller,

wherein said second DMA controller arbitrates data transfer between said second memory and said first buffer memory and data transfer between said second memory and said second buffer memory.

11. An image input/output device as defined in claim 7, wherein said processor is substituted by a plurality of processors.

12. An image input/output method utilizing an image input/output device, the image input/output device including: a first bus; a processor operable to connect with the first bus; a first DMA controller operable to connect with the first bus; a second bus; a second DMA controller operable to mutually connect the first bus and the second bus; a first connecting unit including a synchronizing signal detector and a first buffer memory and operable to connect with the second bus; and a second connecting unit including a synchronizing signal generator and a second buffer memory and operable to connect with the second bus, a first memory connected to the first bus and accessible by the processor and the first DMA controller, and a second memory connected to the second bus and accessible by the second DMA controller, the image input/output method comprising:

detecting effective image data from an externally inputted image signal by the synchronizing signal detector of the first connecting unit and storing the effective image data to said first buffer memory;

generating image output signal by inserting a synchronizing signal to image data stored in said second buffer memory, and sending externally the image output signal;

arbitrating, by the second DMA controller, data transfer between the second memory and the first buffer memory and data transfer between the second memory and the second buffer memory; and

arbitrating, by the first DMA controller, data transfer between the first memory

and the second memory through the second DMA controller.

13. An image input/output method utilizing an image input/output device, the image input/output device including: a first bus; a processor operable to connect with the first bus; a first DMA controller operable to connect with the first bus; a second bus; a second DMA controller including a DMA arbiter and a transfer output buffer memory and a transfer input buffer memory, the second DMA controller being operable to mutually connect the first bus and the second bus; a first connecting unit including a synchronizing signal detector and a first buffer memory and operable to connect with the second bus; and a second connecting unit including a synchronizing signal generator and a second buffer memory and operable to connect with the second bus, a first memory connected to the first bus and accessible by the processor and the first DMA controller, and a second memory connected to the second bus and accessible by the second DMA controller, the image input/output method comprising:

arbitrating, by the DMA arbiter upon receipt of data transfer request from the first connecting unit, data transfer between the first buffer memory and the second memory via the second bus;

arbitrating, by the DMA arbiter upon receipt of data transfer request from the second connecting unit, data transfer between the second buffer memory and the second memory via the second bus;

arbitrating, by the DMA arbiter upon receipt of data transfer request from the first DMA controller, data transfer from the second memory to the first memory via the transfer output buffer memory; and

arbitrating, by the DMA arbiter upon receipt of data transfer request from the first DMA controller, data transfer from the first memory to the second memory via the transfer input buffer memory.